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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Allen et al.

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Examiner: Siek, Vuthe

For: THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE
YIELD AND RELIABILITY OF VLSI DESIGNS

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF REPLACEMENT DRAWING SHEETS

Sir:

Submitted herewith are seven sheets of replacement drawing sheets comprising Figures 1-11. Please replace the drawings originally filed with the accompanying formal drawings. Approval and acknowledgment of receipt are respectfully requested.

Respectfully Submitted,

Frederick W. Gibb, III
Reg. No. 37,629

Date: 4/6/05
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April 6, 2005

Frederick W. Gibb, III